REMARKS

Reconsideration and allowance of the subject application are respectfully requested. Claims 1-17 are all the claims pending in the application. Applicant respectfully submits that the pending claims define patentable subject matter.

Applicant herein amends the claims for clarity. No new matter has been added.

Drawing Objections

The drawings are objected to under 37 C.F.R. 1.83(a). The Examiner asserts that the order of writing meta-information and data as recited in claims 2, 3, 12, and 13 is not shown. Applicant respectfully disagrees with the Examiner's position.

As shown, for example, in FIGS. 8a and 8b, operations (1) and (2) may either occur simultaneously (as indicated by the dashed line of operation (2)), or sequentially, (again, as indicated by the dashed line of operation (2)). Applicant submits that the dashed line indicates an optional ordering of operations. That is, operation (1) and (2) may either occur simultaneously or sequentially. Accordingly, Applicant respectfully requests that the Examiner withdraw the objection to the drawings.

Claim Rejections Under 35 U.S.C. § 112

Claims 2, 3, 12, and 13 stand rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. Specifically, the Examiner alleges that the claimed feature of claims 2 and 12 reciting "The method as claimed in claim 11, wherein the meta-

information is written after the data of the logical block is written," is not supported in the specification. Applicant respectfully traverses this rejection.

As pointed out above, as shown, for example, in FIGS. 8a and 8b, operations (1) and (2) may either occur simultaneously (as indicated by the dashed line of operation (2)), or sequentially, (again, as indicated by the dashed line of operation (2)). Applicant submits that the dashed line indicates an optional ordering of operations. That is, (1) and (2) may either occur simultaneously or sequentially. Further, page 15, paragraph [95] of the specification, for example, describes writing data in operation (1). Similarly, page 15, paragraph [96] of the specification, for example, describes writing flash memory state information (i.e., meta information) in operation (2).

In other words, the cited portion, along with the drawings, disclose both the claimed features "wherein the meta-information is written after the data of the logical block is written," and, with regard to claims 3 and 13, "wherein the data and meta-information of the logical block are simultaneously written." Accordingly, Applicant respectfully requests that the Examiner withdraw this rejection of claims 2, 3, 12 and 13.

Claims 1-17 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite. With regard to independent claims 1 and 11, the Examiner asserts the claimed feature "if a previous write operation has not been performed for the logical block" is unclear. In particular, the Examiner asserts that it is unclear whether the claimed feature means that there has previously been a write operation to the logical block, or if there was previously a write operation issued to the logical block but for some reason it was not performed. Applicant

submits that the claimed feature is clear as to its meaning. The phrase "if a previous write operation has not been performed for the logical block" is not limited to either situations noted by the Examiner. That is, "if a previous write operation has not been performed" comprises any situation where a previous write operation has not been performed, not just the two scenarios set forth by the Examiner. Thus, Applicant submits that the meaning of the claimed feature is definite in that it comprises any situation where a previous write operation has not been performed. Accordingly, Applicant requests that the Examiner reconsider and withdraw this rejection.

With regard to claims 6-10 and 12-17, Applicant submits that the claim amendments submitted herein obviate the informalities noted by the Examiner, and therefore respectfully requests that the Examiner withdraw these claim rejections.

Claim Rejections Under 35 U.S.C. § 102

Claims 1, 3, 4, 11, 13 and 14 stand rejected under 35 U.S.C. 102(b) as being anticipated by Conley (US 2002/0099904). Applicant respectfully traverses this rejection.

Independent claim 1 recites, in part:

> wherein if a write operation is requested for a logical block number of the flash memory, the flash memory controller is configured to write data and meta-information in a physical block corresponding to a logical block with the logical block number if a previous write operation has not been performed for the logical block, and the flash memory controller is configured to perform a write operation for writing the data and the meta-information

> allocated to the logical block in a new physical block without changing flash memory state information written in a previous physical block corresponding to the logical block if the previous write operation has been performed for the logical block.

Thus, claim 1 requires, *inter alia*, that if the previous write operation for the logical block had completed, the flash controller writes the data and the meta-information in a new physical block without changing flash memory state information written in a previous physical block.

Conley, on the other hand, merely discloses a physical block[1] having a logical block number[2] and a time stamp.[3] The time stamp used in Conley only indicates a time at which data was last written to the physical block. Moreover, a time stamp is different from state information since a time stamp indicates time, whereas state information indicates a status.

Conley fails to disclose anything related to state information, i.e., a status of the physical block itself. Indeed, Conley is silent on any such feature. Thus, Applicant respectfully submits that Conley fails to teach or suggest without changing flash memory state information written in a previous physical block, as claim 1 requires.

Accordingly, Applicant submits that independent claim 1 is patentable over Conley for at least these reasons. Similarly, Applicant submits that independent claim 11 is patentable over Conley for reasons analogous to those stated above regarding claim 1. Further, Applicant

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[1] See e.g., Conley, FIG. 8, element 35.

[2] See e.g., Conley, FIG. 8, element 41.

[3] See e.g., Conley, FIG. 8, element 43.

submits that claims 3, 4, 13 and 14 are patentable over Conley, at least by virtue of their respective dependency on claims 1 and 11.

Claim Rejections Under 35 U.S.C. § 103

Claims 5, 6, 8-10, 15, and 17 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Conley (cited supra) in view of Kim et al. (US 6,381, 176; hereinafter "Kim"). Applicant respectfully traverses this rejection.

Kim fails to cure the deficiency of Conley noted above regarding independent claims 1 and 11. In particular, Kim fails to teach or suggest the claimed feature of "if the previous write operation for the logical block had completed, the flash controller writes the data and the meta-information in a new physical block without changing flash memory state information written in a previous physical block corresponding to the logical block."

In Kim, the status of previous blocks are changed regardless of whether an empty block exists. For example, in step 613,[4] the status of the previous block is changed. Likewise, the status of the previous block is changed during the reclaim operation 617.[5] Thus, Kim fails to teach or suggest the above-noted feature of the claimed invention.

Accordingly, Applicant submits that the combination of Conley and Kim fail to teach or suggest all of the claimed features of independent claims 1 and 11. Therefore, Applicant submits

[4] See Kim, FIG. 6.

[5] See Kim, col. 7, lines 49-58.

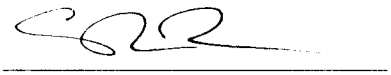
that claims 5, 6, 8-10, 15, and 17 are patentable over the cited references, at least by virtue of their respective dependency on claims 1 and 11.

Conclusion

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,



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